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PATENT APPLICATION
Attorn y Dock t No. D/A1102

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Paul A. Hosier et al.
Application No.: 09/802,792
Filed: 3/8/2001
Examiner: Seung C. Sohn
Confirmation No.: 8347
Art Unit: 2878
Title: **COLOR FILTER CONFIGURATION FOR A SILICON WAFER TO BE DICED INTO PHOTOSENSITIVE CHIPS**

CERTIFICATE OF MAILING

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Francie S. LePore

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Sir:

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

LETTER

Enclosed herewith is an original and two copies of Appellants' Brief on Appeal in the above-identified application. An oral hearing is not requested.

Please charge the fee for filing of the Appeal Brief to Xerox Corporation, Deposit Account No. 24-0025. Two duplicate copies of this letter are enclosed.

Respectfully submitted,

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September 10, 2003
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#13 PB
9/30/03

PATENT APPLICATION

Attorney D cket No. D/A1102

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APPELLANTS' BRIEF ON APPEAL

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1. REAL PARTY OF INTEREST

Xerox Corporation, assignee of the present patent application.

2. RELATED APPEALS AND INTERFERENCES

There are no related appeals and interferences.

3. STATUS OF CLAIMS:

Claims 1-3 and 6-30 are rejected.
Appellants are appealing all the rejected claims.

4. STATUS OF AMENDMENTS:

The Amendment filed in response to the Final Rejection has been entered.

5. SUMMARY OF INVENTION:

The present application relates to photosensor chips, as would be used, for example, in a digital scanner or digital camera. The photosensor chip typically defines, on a main surface thereof, a large number of discrete photosensitive areas, each of which includes associated circuitry which reads out a signal related to the light falling on the photosensitive area at a given time. Thus, when a light image is focused on the chip, readings can be output from the chip to yield a set of image signals.

It is common that photosensor chips are made in generally the same way as any silicon integrated circuit chip, in that circuitry for a large number of independent chips is created in a silicon wafer. After the circuitry has been laid down in the

silicon wafer, the silicon wafer is cut up or "diced" along the borders between the circuitries of individual chips therein. A wafer is thus "diced" into individiual chips.

One common attribute of photosensor chips is one or more light-transmissive layers, typically made of acrylic or polyimide, which are disposed on the silicon of the chip. Ordinarily, such light-transmissive layers act as light filters for the photosensitive areas on each chip, such as to filter out IR light from the photosensitive areas, or to facilitate separate primary-color-sensitive areas on each chip. In many applications, the light-transmissive layers are placed on the wafer before the dicing process.

The present application relates to using such a "light-transmissive planar layer" over a wafer or a chip, but for a purpose different from its typical, purely optical use. In the invention as claimed, a light-transmissive planar layer is provided over a chip, in a way that a portion of the layer extends over a portion of the groove which defines an edge of the chip.

Of the claims under rejection, claims 1, 11, and 20 are independent. Although the various claim sets are directed to, respectively, a chip, an apparatus having a chip, and a wafer (from which chips can immediately be diced), at least one feature is common to all of the independent claims: the chip includes a **portion of a groove** which defines an edge of the chip. A light-transmissive planar layer extends **over** this portion of the groove.

An embodiment of this claimed feature is shown in the specification as filed at Figure 3 for a chip which has not yet been diced from a wafer. Figure 3, shown here, is a cross-sectional view through a wafer, at a site forming an edge of a chip. In the wafer, the edge of each chip is defined by a relatively deep groove 70. A planar or planarization layer 72, which is light-transmissive, is then placed over the whole wafer and in effect fills up each groove 70; a further layer such as 74 can in turn be placed on top of layer 72. In the dicing process, the wafer is sawn through line 71, which is located within deep groove 70. Because the planar layer 72 extends over the portion of the groove 70, such as shown as the material to the right of cut line 71, the top surface of the chip is made planar over the portion of the groove 70 which remains as part of the diced chip:

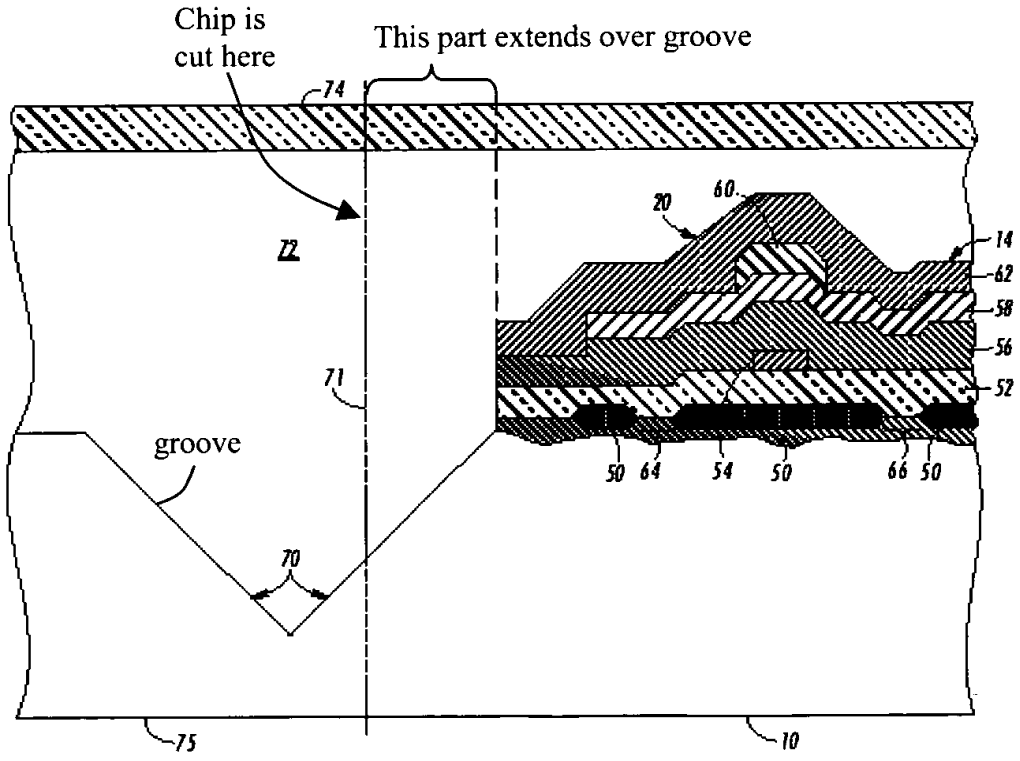


FIG. 3

The practical advantage provided by this chip and wafer configuration, especially in the sense that the planarization layer 72 is *left in the groove* 70 at the dicing step, is given at pages 2 and 8 of the specification as filed (emphases added):

> One problem concerns the inadvertent ripping or other damage to the cured filter layers when the wafer is diced into individual chips: **the relatively thin translucent filter layer**, particularly at the photosensors toward either end of the chip, **can be torn by the action of a saw blade.**
> * * *
> [With the present invention, w]hen a wafer is diced, such as along a groove 70, [because of] the fact that each filter layer 74 is disposed over and supported by clear [planar] layer 72, which itself takes up most of the void formed by the groove 70, **the filter layer 74 exhibits very little damage or tearing**, especially in the portions thereof around any photosites 14.

In short, the planarizing layer 72 being *allowed to remain within the groove 70* prevents or lessens damage to a filter layer during a dicing process.

6. ISSUES:

Whether claims 1, 6-11, 14-20, 22-24, 26, and 28-30 are unpatentable under 35 USC 102(b) as being anticipated by Koizumi '892.

Whether Claims 2, 12, and 21 are unpatentable under 35 USC 103 over Koizumi.

Whether Claims 3, 13, and 25 are unpatentable under 35 USC 103 over Koizumi, as applied to their respective independent claims, and further in view of Jedlicka.

7. GROUPING OF CLAIMS:

For each of the rejections, the claims do not stand or fall together.

8. ARGUMENT:

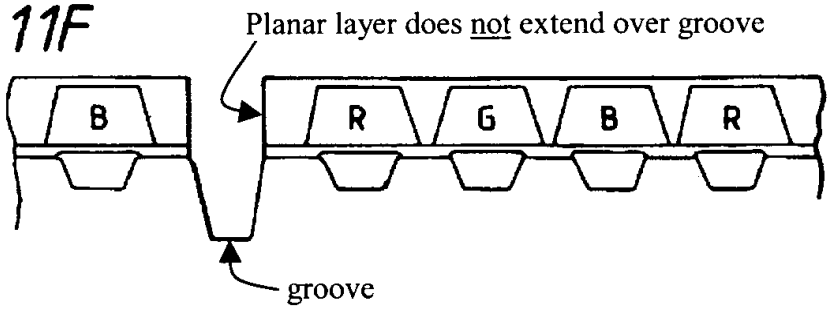
Claims 1, 6-11, 14-20, 22-24, 26, and 28-30 have been rejected under 35 USC 102(b) as being anticipated by Koizumi '892.

In the rejection, as an instance in the prior art of "the planar layer extending over the groove portion," there is cited column 2, lines 57-58 of Koizumi. The cited portion, it must be noted, is part of a larger discussion of a process described in the reference. However, close examination of the *entire* method and its resulting product show key differences between the reference and the claims, as noted at Column 2, lines 56-67 of Koizumi (emphasis added):

> In order to eliminate steps on the device surface, the entire surface of the device is coated with a transparent resist [FIG. 11C]. Then, coating and patterning for red (96), blue (98), and green (99) color filters are sequentially repeated, thus forming color filters [FIG. 11D]. Furthermore, in order to protect the respective filters, a passivation layer is formed on the entire surfaces of the respective color filters [FIG. 11E]. **Finally, a transparent resin in each scribe region is removed** [FIG. 11F]. **Thereafter,** respective solid-state image pickup **chips are cut along the scribe regions** using, e.g., a dicing cutter.

An illustration of the described principle is shown in Figure 11F of Koizumi. There is unambiguously ***no*** "planarization layer" ***in the groove*** when the wafer is about to be diced, because, as clearly stated above, the layer has been **removed** prior to dicing:

FIG. 11F



It is perfectly clear by the above passage and Figure 11F of Koizumi, immediately before the dicing step, the transparent resist, or the light-transmissive layer, is ***compl t ly remov d from th groove C***. Therefore, **no part** of the light-

transmissive layer in Koizumi can be said to *extend into the area* corresponding to groove C in either the wafer (immediately pre-dicing) or the finished chip, as recited in every independent claim.

Independent **claims 1 and 11** both positively recite that the light-transmissive planar layer extends over the groove portion at the edge of the chip, a structure that would clearly be impossible to achieve with the wafer as shown in Figure 11F of Koizumi, where the planarizing layer is clearly *removed* from the groove before the wafer is diced into chips. Independent **claim 20**, directed to a wafer, has been amended to recite positively that the wafer as claimed is suitable "for immediate dicing" into at least one chip, which means that the light-transmissive layer in the groove *remains in the groove* up to the point of dicing.

In the Final Office Action, the assertion is made that the fact Koizumi removes the planarization layer before dicing has "nothing to do with the rejection since the examiner rejected the claim[s] using the Figs. 11C and 11D [of Koizumi], which show the chip before removing the light-transmissive layer." However, the *precise wording* of each independent claim distinguishes the claimed invention from the disclosure in Figs. 11C and 11D of Koizumi: the independent claims at issue relate to either an already-diced ***chip***, a ***chip*** as part of a larger apparatus, or to a wafer *"suitable for **immediate** dicing"* into a ***chip***.

The disclosed structures in Figs. 11C and 11D of Koizumi do not relate to a chip nor to a wafer suitable for immediate dicing. In the cited figures, we are looking at, purely, a *wafer*— **not a chip**, because a chip is a wafer which has been diced, and the wafer in Figs. 11C and 11D *has not yet been diced*. Therefore, the cited Figures do not teach the invention of claims 1 or 11, which relate unambiguously to a **chip**.

Nor are the disclosed structures in Figs. 11C and 11D of a wafer "suitable for immediate dicing" into a chip, as in independent claim 20: by the disclosure of Koizumi itself, the structure of Figs. 11C and 11D must go through *at least* the steps of Figs. 11E-F (which describe the *removal* of the planarization layer) before any dicing is contemplated. Therefore, the specific cited art, Figs 11C and 11D of

Koizumi, does not teach the invention of claim 20: a wafer "suitable for immediate dicing."

Claims 2, 12, and 21 are rejected under 35 USC 103 over Koizumi. Claims 3, 13, and 25 are rejected under 35 USC 103 over Koizumi, as applied to their respective independent claims, and further in view of Jedlicka, which discloses the use of acrylic for a filter layer. These claims are deemed allowable as being dependent upon their respective independent claims, the patentability has been argued above.

Based on the foregoing reasons, the Board of Appeals is respectfully urged to reverse the Examiner on each of the rejections.

Respectfully submitted,

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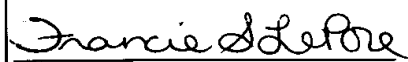 Date: 9/10/2003

Francie S. LePore

9. APPENDIX:

CLAIMS APPEALED:

1. A photosensitive chip for use in an imaging apparatus, comprising:

a main surface, having at least one photosite thereon, the main surface defining an edge;

a groove portion defined at the edge;

a light-transmissive planar layer disposed over the main surface, the planar layer forming a planar surface substantially parallel with the main surface, the planar layer extending over the groove portion; and

a light-transmissive filtering layer disposed over the planar layer.

2. The chip of **claim 1**, the planar layer comprising acrylic.

3. The chip of **claim 1**, the filtering layer comprising acrylic.

6. The chip of **claim 1**, the planar layer being substantially transmissive of visible light, and the filtering layer being transmissive of a predetermined range of wavelengths of light.

7. The chip of **claim 1**, the filtering layer comprising a first portion transmissive of a first predetermined range of wavelengths of light and a second portion transmissive of a second predetermined range of wavelengths of light.

8. The chip of **claim 7**, the first portion being disposed over a first photosite and the second portion being disposed over a second photosite.

9. The chip of **claim 7**, the first portion being disposed over a first set of photosites and the second portion being disposed over a second set of photosites.

10. The chip of **claim 1**, further comprising a ridge defined on the main surface between the photosite and the groove portion.

11. An imaging apparatus having a first photosensitive chip, the chip comprising:

a main surface, having at least one photosite thereon, the main surface defining an edge;

a groove portion defined at the edge;

a light-transmissive planar layer disposed over the main surface, the planar layer forming a planar surface substantially parallel with the main surface, the planar layer extending over the groove portion; and

a light-transmissive filtering layer disposed over the planar layer.

12. The apparatus of **claim 11**, the planar layer comprising acrylic.

13. The apparatus of **claim 11**, the filtering layer comprising acrylic.

14. The apparatus of **claim 11**, the planar layer being substantially transmissive of visible light, and the filtering layer being transmissive of a predetermined range of wavelengths of light.

15. The apparatus of **claim 11**, the filtering layer comprising a first portion transmissive of a first predetermined range of wavelengths of light and a second portion transmissive of a second predetermined range of wavelengths of light.

16. The apparatus of **claim 15**, the chip including a plurality of photosites on the main surface thereof, the first portion being disposed over a first set of photosites on the first chip and the second portion being disposed over a second set of photosites on the first chip.

17. The apparatus of **claim 11**, further comprising a second photosensitive chip, the second chip having a planar layer and a filtering layer arranged substantially similarly to the first chip.

18. The apparatus of **claim 11**, further comprising a second photosensitive chip, the second chip having a plurality of photosites thereon, the first chip and the second chip being arranged to yield a single functional array of photosites.

19. The apparatus of **claim 18**, the second chip having a planar layer and a filtering layer arranged substantially similarly to the first chip.

20. An integrated circuit wafer, comprising:

a first chip area defined in a main surface of the wafer, the first chip area including structure related to a first photosite;

a groove defined in the wafer, the groove defining at least one edge of the first chip area; and

a light-transmissive planar layer disposed over the main surface, the planar layer forming a planar surface substantially parallel with the main surface, the planar layer extending over the groove.

21. The wafer of **claim 20**, the planar layer comprising acrylic.

22. The wafer of **claim 20**, the planar layer further disposed over the first photosite.

23. The wafer of **claim 20**, further comprising a filtering layer disposed over the planar layer.

24. The wafer of **claim 23**, the filtering layer extending over the first photosite and over the groove.

25. The wafer of **claim 23**, the filtering layer comprising acrylic.

26. The wafer of **claim 20**, further comprising a second chip area defining a second photosite, the filtering layer further extending over the second photosite.

27. The wafer of **claim 20**, the filtering layer comprising a first portion transmissive of a first predetermined range of wavelengths of light and a second portion transmissive of a second predetermined range of wavelengths of light.

28. The wafer of **claim 20**, the first chip area including a first plurality of photosites, the first portion of the filtering layer being disposed over a first set of photosites on the first chip area and the second portion of the filtering layer being disposed over a second set of photosites in the first chip area.

29. The wafer of **claim 28**, further comprising a second chip area defining a second plurality of photosites, the second chip area including a second plurality of photosites, the first portion of the filtering layer being disposed over a first set of photosites on the second chip area and the second portion of the filtering layer being disposed over a second set of photosites in the second chip area.

30. The wafer of claim 20, the first chip area further comprising a ridge defined on the main surface between the photosite and the groove portion.